An all-chromium single electron transistor: A possible new element of single electronics

L. S. Kuzmin[a] and Yu. A. Pashkin[b]
Physikalisch-Technische Bundesanstalt, D-38116 Braunschweig, Germany and Department of Physics, Chalmers University of Technology, Gothenburg S-41296, Sweden

A. N. Tavkhelidze,[c] F.-J. Ahlers, T. Weimann, D. Quenter, and J. Niemeyer
Physikalisch-Technische Bundesanstalt, D-38116 Braunschweig, Germany

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The realization of an all-chromium single electron tunneling (SET) transistor is reported. Chromium was chosen as a normal metal with small grain structure forming the oxide layer with a low potential barrier and great chemical and thermal stability. The transistor showed classical I-V curves with an offset voltage of 450 μV and an amplitude of gate modulation of 160 μV. Fitting a tunnel current expression in the experimental I-V curve gave a height of the potential barrier $\phi=170$ meV and a width of the barrier $d=16$ Å. The SET transistor showed a charge sensitivity of 7×10^{-4} $e/\mathrm{Hz}^{1/2}$ at 10 Hz. © *1996 American Institute of Physics.* [S0003-6951(96)03220-2]

A new class of devices based on single charge tunneling phenomena has been intensively developed in recent years (see Refs. 1 and 2 for reviews). These devices operate at low temperatures T and comprise tunnel junctions with a small capacitance $C \gg e^2/k_B T$, where e is the electron charge. The devices have demonstrated unique properties, including sub-electron charge sensitivity, the possibilities of manipulating electrons one by one, and of creating a current standard. However, the main drawback of such devices is their instability due to the shift of a background charge. Several attempts have already been made to eliminate this instability by fabricating SET transistors on various substrates (Si, SiO_2 and Al_2O_3)[3] and by using different electrode materials[4] but have not met with much success. It is clear that testing new materials for tunnel junctions and substrates could be very useful in bringing about an improvement of the noise properties of these devices. Another purpose is to find a normal metal instead of the commonly used superconducting aluminum, in which case we do not need to suppress the superconductivity by a magnetic field. We decided to use chromium for several reasons. This material showed very good stability, excellent adhesion properties, and small grain structure when we used very thin (6 nm) films of Cr as resistors.[5] Chromium forms a stable oxide layer which can be used for the fabrication of tunnel junctions.[6] The low potential barrier between the chromium oxide and other materials leads to comparatively thicker oxide barrier for the same tunnel resistance, and, so, to a smaller capacitance for the same dielectric constant, and probably to more stable junctions. The purpose of this work was to fabricate SET transistors using $Cr–Cr_2O_3–Cr$ tunnel junctions and investigate the parameters of the tunnel barrier and noise properties of the transistors.

The $Cr–CrO_x–Cr$ tunnel junctions were fabricated using electron beam lithography and shadow evaporation technique. We used a double-layer resist composed of PMMA and copolymer (PMMA-PMAA) for an e-beam mask as for Al junctions. However, we had difficulty with the evaporation of Cr as its melting point is higher than that of Al. When the total thickness of evaporated Cr was 50 nm, the mask cracked and samples could not be fabricated successfully. We then reduced the thickness of both electrodes and evaporated the top one in several steps. The base Cr layer of 10 nm thick was evaporated from a thermal boat at a rate of 0.05 nm/s on an oxidized silicon substrate. The tunnel barrier was formed by thermal oxidation in an oxygen atmosphere at a pressure of 2×10^4 Pa for 15 h at room temperature. The formation of the tunnel barrier was the most important step. For the normal operation of the transistor, one should achieve a junction resistance R high enough so that $R \gg R_Q \equiv h/4e^2 \approx 6.47$ kΩ. For a typical junction area of $S=0.01$ $\mu\mathrm{m}^2$ we could not get a value of the resistance high enough. A longer oxidation time did not result in an increase in resistance. The reason for this is a saturation level of Cr_2O_3 of the order of 1 nm formed at room temperatures.[7] The proper resistance was achieved by reducing the junction area to 0.003 $\mu\mathrm{m}^2$ for transistor configuration. Due to different geometry, the area of single junctions made on the same substrate was not reduced to the same level and all investigations were made for the transistor. The top electrode was 20 nm thick and deposited at the same rate as the base electrode but in two steps with a 5 min interval. Electrical contacts to the chip were made by directly connected pogo pins to Cr contact pads. Such contacts produced some instability in transistor operation. Silver paste on the contact pads helped to create more stable contacts. The measurements were made in a dilution refrigerator at temperatures around 50 mK.

A I-V curve of a Cr transistor is shown in Fig. 1(a). The I-V curve has the classical Coulomb blockade shape of a normal metal transistor. The I-V curve at higher bias voltages referred to one junction is shown in Fig. 1(b). At higher voltages it has a noticeable curvature that was not observed for Al junctions. The reason for this curvature is the suppression of the tunnel barrier at voltages lower than for Al due to the lower potential barrier for Cr tunnel junctions. The parameters of the potential barrier, the height φ and the width d, were determined from the I-V curve at higher bias volt-

[a]Current address: Laboratory of Cryoelectronics, Moscow State University, Moscow 119899, Russia. Electronic mail: kuzmin@fy.chalmers.se
[b]Current address: Lebedev Physical Institute, Russian Academy of Sciences, Moscow 117924, Russia.
[c]Current address: Laboratory of Cryoelectronics, Moscow State University, Moscow 119899, Russia.

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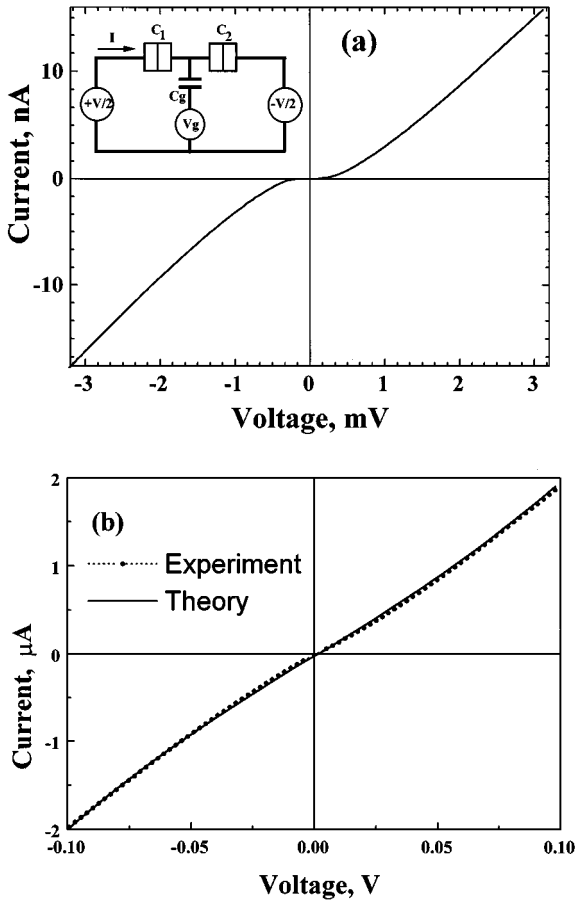

FIG. 1. (a) The $I-V$ curve of the SET transistor with $Cr-CrO_x-Cr$ tunnel junctions at $T=50$ mK. (b) The experimental and theoretical $I-V$ curves at higher bias voltages. The parameters of the potential barrier, the height φ and the width d, were determined for the best fitting of the theoretical $I-V$ curve calculated using formula (1) for the tunneling current through the barrier of a rectangular shape.

ages [Fig. 1(b)] using a formula derived by Simmons[8] for the tunneling current through the barrier of a rectangular shape:

$$I=6.2\times10^{10}\ \ S/d^2[(\varphi-V/2)\exp(-1.025d(\varphi-V/2)^{1/2}] -(\varphi+V/2)\exp[-1.025d(\varphi+V/2)^{1/2}], \quad (1)$$

where φ is in eV, d is in Å and S is in cm^2. Due to the high dielectric constant of Cr_2O_3 [$\varepsilon=12$ (Ref. 6)], the image force correction was not taken into account. We also assumed that both junctions of the transistor are identical. For a correct fitting of the expression (1) to the experimental I-V curve, the offset voltage V_{off} was subtracted from the I-V curve and region near the beginning of coordinates ($\cong$3 mV) was not taken into account for comparison with the theory. The best fit of (1) to the experimental I-V curve gave the following parameters of the barrier: $\varphi\cong170$ meV and $d\cong16$ Å. The height of the barrier is lower than for Al ($\varphi\cong1.6$–2.4 eV) but higher than for lead-alloy junctions with a Cr_2O_3 barrier ($\varphi\cong20$ meV).[6] For a single-electron transistor with barrier suppression, the new type of peculiarities on the I-V curve was predicted theoretically.[9] We checked I-V curves of the transistor using a derivative techniques but did not find any trace of this effect. The most probable reason is still relatively high value of potential barrier (170 mV) in comparison with the scale of charging effects ($\cong$0.5 mV).

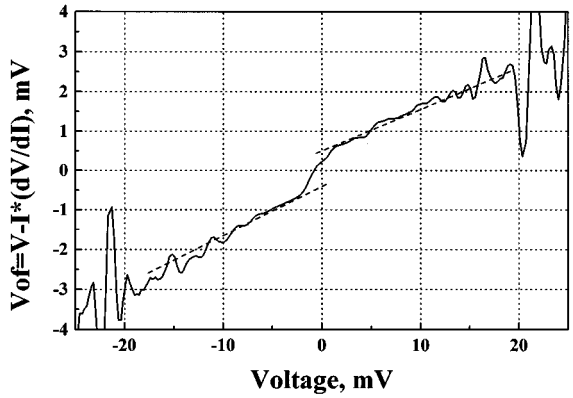

FIG. 2. Offset voltage of the transistor determined using the derivative of the $I-V$ curve.

Junction capacitances were determined using two methods: through an offset of voltage asymptotes of the I-V curve and through the gate modulation curve of the transistor. Determining the parameters through the offset voltage has two complications. The external impedance is changed at moderate voltages due to the transition from ''global'' to ''local rule'',[10,11] and the potential barrier is suppressed at higher voltages. We can expect a linear I-V curve in the region between this two effects, somewhere around 10–20 mV. To determine more accurately the change of the offset voltage at different bias voltages, we calculated $V_{of}=V-dV/dI\times I$[12] from the experimental data (Fig. 2). The curve is not zero at $V=0$ due to intrinsic offset of the measurement system. The curve has no clear plateau at voltages higher than 10 mV. More than that, it is also apparent that V_{of} has more than doubled at 10 mV in comparison with V_{of} at small voltages, which cannot be explained by the change in the external impedance. Analyzing the possible influence of suppression of the potential barrier on offset voltage, we calculated the V_{of} using (1) on assumption of rectangular potential barrier with an estimated φ and d of the barrier. The estimations show the influence of this effect only after 20 mV and could not explain monotonic increasing of V_{of} at lower bias. We see unique explanation of such dependence of V_{of} in the nonuniformity of the barrier that gives different values of φ for different parts of the barrier. For such a barrier one can expect nonlinearity of the I-V curve at lower voltages. Previously estimated parameters of the barrier should be considered as average values. Extrapolating V_{of} back to zero voltage where the transistor should have no influence of both effects of external impedance and barrier suppression, the value of the offset voltage can be estimated as $V_{off}\cong450$ μV. The offset voltage is related to the total capacitance of the transistor $C_\Sigma=C_1+C_2+C_g$ as $V_{off}=e/C_\Sigma$ that gives $C_\Sigma=0.36$ fF.

The gate modulation characteristic of the transistor is shown in Fig. 3. A biased current was chosen for the most stable operating point with nearly maximum amplitude of modulation. The device parameters can be deduced from the period and slopes of the modulation curve[13] using a formula: $C_{1,2}=e/(dV/dV_g)_{p,n}/\Delta V_g$, where ΔV_g is the period of the gate modulation and symbols p and n denote positive and negative slopes of the modulation dependence. The estimation results in $C_1=0.33$ fF, $C_2=0.45$ fF, $C_g=16$ aF with a

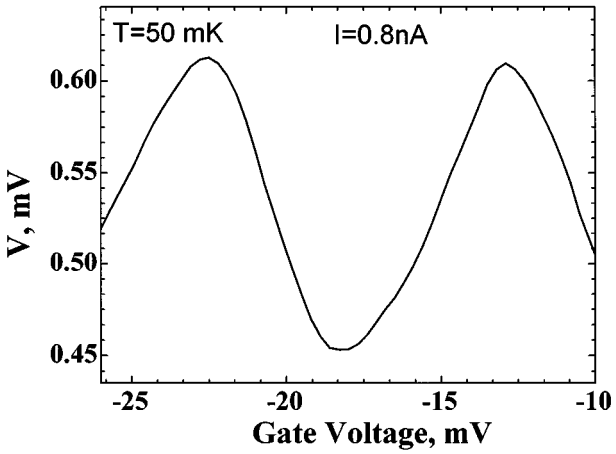

FIG. 3. Output voltage as a function of the gate voltage at a fixed bias current near the Coulomb blockade region.

total capacitance of $C_\Sigma = 0.78$ fF. The total capacitance is twice as large as C_Σ estimated from the offset voltage. Such a discrepancy is typical for transistor experiments.[14] The reason for the higher offset voltage could be double tunneling through the barrier of each junction.[15] Such double tunneling inside the junctions results in an additional offset voltage but does not increase an amplitude of the gate modulation. The effect is more noticeable for junctions with higher resistance. Dependence of the offset voltage on junction resistance can be seen for large statistics of the junctions in Ref. 16.

The noise measurements of the transistor were made using a spectrum analyzer over a wide frequency range from 0.2 Hz up to 1 kHz (Fig. 4). The input charge noise was defined using a formula $Q_N = C_g V_N (dV_g/dV)$ where V_N is voltage noise measured at the output of transistor. Below 100 Hz, the noise referred to the input charge showed a $1/f^{1/2}$ spectrum that is typical for the two-level charge trap fluctuations.[17] The peak at 2.3 Hz was due to mechanical vibrations of the sample holder in a top loading cryostat. Two peaks at 50 and 100 Hz were due to the line influence. Two peaks around 230 and 450 Hz were stable and connected to transistor operation but their origins were not clear. Noise measurements made on different days produced different results and showed a tendency for the noise to diminish with time. One of the best measurements showed a charge sensitivity of $Q_N \cong 7 \times 10^{-4} e/\mathrm{Hz}^{1/2}$ at 10 Hz which is of the same order as for aluminum junctions. The reason for such an unstable transistor operation could be an imperfect tunnel barrier consisting of a saturated layer of Cr_2O_3 (about 9 Å) and adsorbed oxygen. This assumption of additionally adsorbed oxygen is supported by the estimated thickness of the barrier which appeared to be higher than the saturation level of Cr_2O_3. We believe that a transistor with a perfect Cr_2O_3 barrier could be created by using substantially higher temperatures (more than 200 °C) for oxidizing the base electrode.[7] Stability of chromium against oxidation opens up new possibilities for direct-writing technology which exposes the sample to the ambient environment between the fabrication of the electrodes. This technology allows us to use independent lithography for each layer and oxidize the base Cr layer at higher temperature after removing the *e*-beam resist of the first layer.

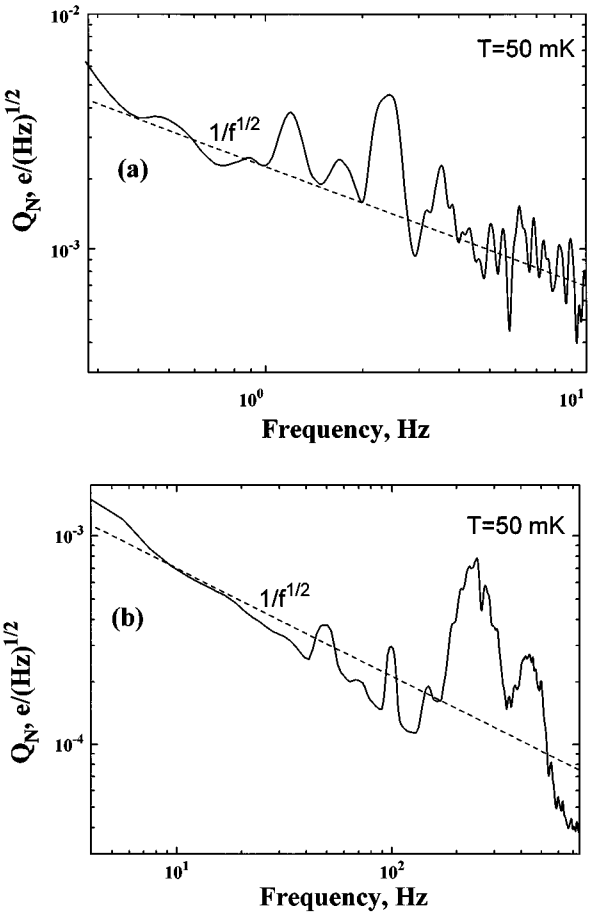

FIG. 4. Charge sensitivity of the SET transistor as a function of frequency for low (a) and high (b) frequency regions.

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