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(54) **METHOD FOR MODIFICATION OF BUILT IN POTENTIAL OF DIODES**

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See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,740,592 A	6/1973	Engdahl et al.	
4,011,582 A	3/1977	Cline et al.	
4,039,352 A	8/1977	Marinescu	
4,063,965 A	12/1977	Cline et al.	
4,686,162 A	8/1987	Stangl et al.	
5,023,671 A	6/1991	DiVincenzo et al.	
5,068,535 A	11/1991	Rabalais	
5,119,151 A *	6/1992	Onda .....	257/14
5,229,320 A	7/1993	Ugajin	
5,233,205 A	8/1993	Usagawa et al.	
5,247,223 A	9/1993	Mori et al.	
5,298,108 A *	3/1994	Miller .....	148/33.4
5,332,952 A	7/1994	Ugajin et al.	
5,336,547 A	8/1994	Kawakita et al.	
5,371,388 A	12/1994	Oda	

(Continued)

FOREIGN PATENT DOCUMENTS

DE 3404137 A1 8/1985

(Continued)

OTHER PUBLICATIONS

Chou et al., "Imprint Lithography with 25 Nanometer Resolution", Science, Apr. 5, 1996, pp. 85-87, vol. 272.

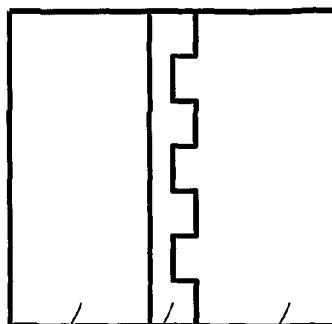
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(57) **ABSTRACT**

In broad terms the present invention is a semiconductor junction comprising a first material (102) and a second material (104), in which a surface of one or both of the junction materials has a periodically repeating structure that causes electron wave interference resulting in a change in the way electron energy levels within the junction are distributed.

**18 Claims, 1 Drawing Sheet**



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