Thermal Management Solutions Using Electron Tunneling Through a Nano-Scale Vacuum Gap

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Abstract. Requirements for cooling and power consumption in space platforms are subject to significantly greater constraints than the requirements for terrestrial applications. Existing cooling systems incorporate various mechanisms including thermoelectric (Peltier) cooling elements, radiative cooling, and phase-change compressor-based systems. This paper outlines an alternative mechanism currently in development called “thermotunneling”. This mechanism exploits electron tunneling across a vacuum gap of ~10nm to effect a temperature differential with high efficiency. When complete, these devices (“Cool Chips”) are expected to offer a compact, lightweight, low maintenance and highly efficient (in excess of 50% of Carnot Efficiency) thermal management solution ideally suited for the needs of aerospace applications. This article was originally published with an incorrect list of authors which is now corrected.

INTRODUCTION

In high earth orbit and interplanetary space, radiative cooling can be an effective general thermal management tool. Many applications, however, require the precise, localized temperature control afforded by active refrigeration solutions. For any aerospace application, a preferred solution should provide cooling in a small, lightweight, low-maintenance package. Thermoelectrics offer a compact, solid-state solution, but low efficiency (Coyle, 1995) has prevented their widespread use.

Cool Chips are a novel solution that rely on an entirely different mechanism known as “thermotunneling”. Thermotunneling refers to the use of electron tunneling to effect a temperature differential between two electrodes. In its simplest form, a thermotunneling diode is simply two electrodes with a spacing of only a few nanometers such that electrons are able to tunnel from one electrode to the other.

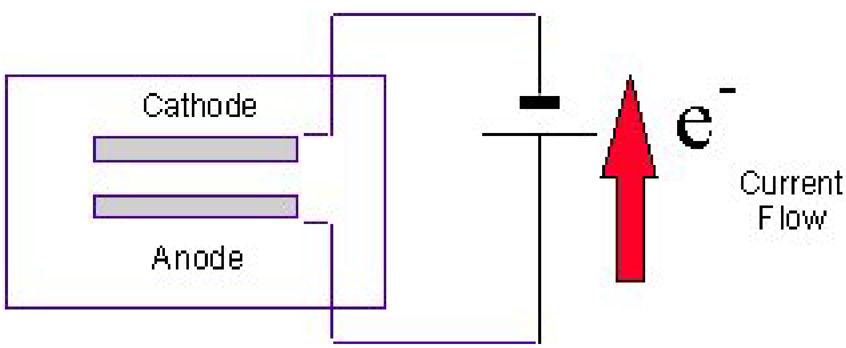

FIGURE 1. Simple Diode Diagram of a Thermotunnel Converter.

Previous attempts to harness electron tunneling as a cooling mechanism have involved the use of a thin film of insulative material separating two metal layers. The use of Superconductor-Insulator-Normal Metal (SIN) structures have been investigated for low-temperature cooling applications (Nahum, 1994), as well as Superconductor-

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Insulator-Normal Metal-Insulator-Superconductor (SINIS) junctions (Luukanen, 2002). As with measurements for Normal Metal-Insulator-Normal Metal (NIN) tunnel junctions (Korotkov, 1994), these constructions suffer from the high thermal conductivity of insulator layers thin enough to permit electron tunneling to take place, and the overall efficiency of such devices is low. Furthermore, attempts to reduce thermal backflow by using many NIN junctions layered in series (Huffman, 1965) have proven very difficult due to the complexity of assembling such devices.

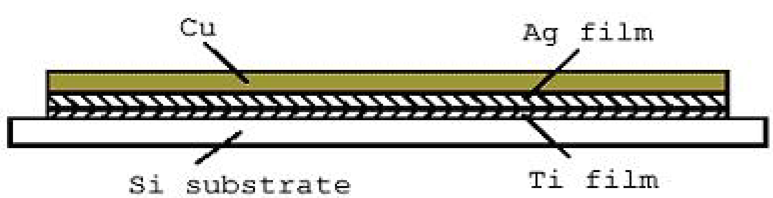
As an alternative to these approaches, our research has focused on the creation of electrodes with a relatively large surface area (on the order of 0.1-1 cm^2) separated by a vacuum gap with a relatively uniform spacing averaging 10 nanometers or less. The creation of this type of Normal Metal-Vacuum-Normal Metal (NVN) junction eliminates phonon coupling between the electrodes (Tavkhelidze, 2001), and avoids the large thermal backpath that saps the efficiency of other solid-state cooling mechanisms (Chen, 2002). Given the extremely high theoretical efficiency of electron tunneling, even after factoring in practical loss terms, Cool Chips are expected to exceed 50% of Carnot Efficiency.

The final goal of our development work (currently in progress) is to integrate materials with a low electron volt work function into the electrodes. Once this work is complete, and performance measurements of working devices have been taken, the remaining tasks will center on packaging finished devices in self-contained modules that incorporate the thermotunneling diode and components to regulate electrode spacing.

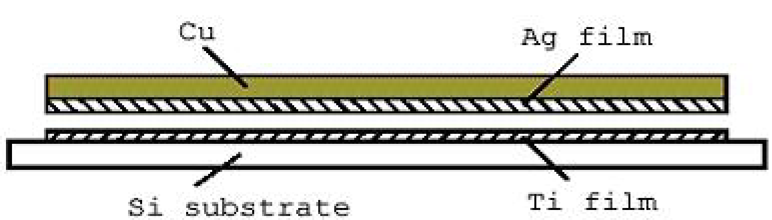
The design of these modules approximates the form factor of the more familiar thermoelectric devices in use today, allowing Cool Chip modules to take advantage of previous engineering efforts to integrate thermoelectric devices for thermal management.

DEVICE CONSTRUCTION

The greatest challenge in the Cool Chip structure is creating the gap between the electrodes. In order for useful electron tunneling to occur, the electrode surfaces must remain less than 10nm apart without coming into contact with each other. Unfortunately, the required micro-scale conformity between the two electrodes exceeds the limits of existing polishing technology. In order to create conformal electrode surfaces, a novel method of surface replication via layered deposition is employed.



(a) Si/Ti/Ag/Cu Sandwich.



(b) Opened Sandwich with Si/Ti and Cu/Ag Electrodes having Conformal Surfaces.

FIGURE 2. Creation of Nanometer-Scale Gap.

The deposition process is fairly straightforward, as illustrated in Figure 2 (above). Beginning with a silicon substrate, a layer of titanium electrode material is deposited through DC magnetron sputtering. A thin layer of silver is then applied to act as a buffer between the two electrodes (in this design, silver is used because of its low adhesion with titanium, and high adhesion with copper). Finally, a layer of copper is deposited on top. The copper layer is subsequently thickened through electrochemical deposition.

Once the top layer is complete, the entire "sandwich" is placed into a specially-constructed test chamber. Inside the chamber, the device is fixed mechanically to a series of piezoelectric positioning elements. Prior to separation, air is evacuated or replaced with an inert gas. By applying thermal and/or mechanical stress to the device, the layers separate cleanly along the junction between the silver and titanium layers. Once separated, we are left with two separate electrodes with precisely matched topographies.

Because the electrode surfaces are matched, they may be brought close enough together to allow electron tunneling over large surface areas without coming into contact with each other. Gap width is regulated via closed-loop capacitive sensors coupled with piezoelectric actuators - in essence a simplified version of the positioning used by scanning electron microscopes. The piezoelectric actuators offer sub-nanometer precision and extremely rapid response, allowing for close control over gap width during operation.

Through optimization of deposition regimes and careful materials selection, high yields of devices with conformal electrode surfaces have been achieved. Further refinements have resulted in devices with low surface curvature and surface roughness – both factors in determining the total available active area for electron tunneling. Local topographical anomalies (peaks and valleys) have a negligible impact on overall performance: valleys create a microscopic void where tunneling is reduced, while peaks are destroyed by bringing the electrodes close enough together for Ohmic current to vaporize them through resistive heating.

Figure 3 (below) is a three-dimensional plot of surface topography showing that average roughness of less than 1 nanometer is achieved.

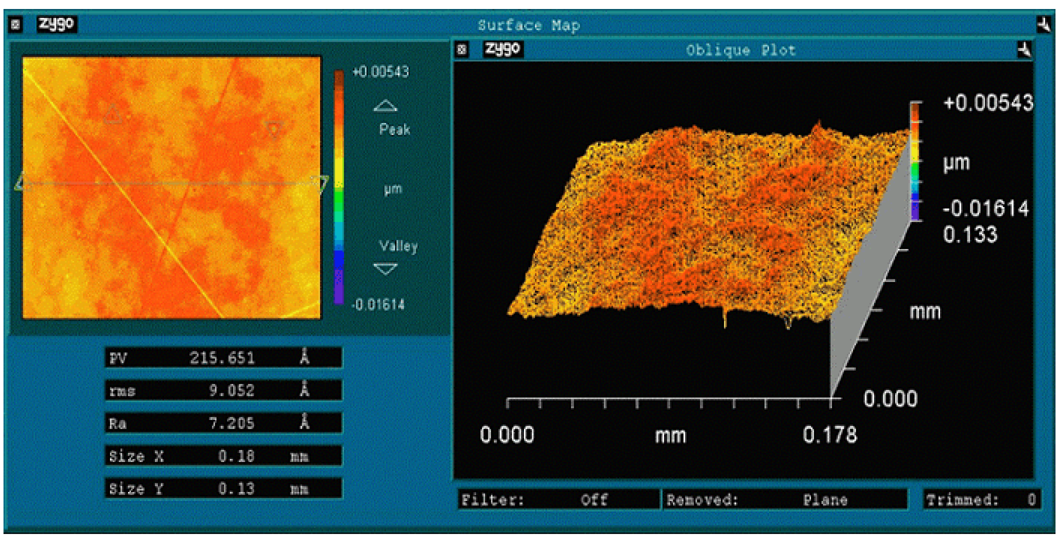


FIGURE 3. Roughness Measurements for a Sample Electrode Surface. Note that Average Roughness (Ra) is Approximately 7 Angstroms.

EVALUATING PERFORMANCE

Until development is completed and detailed measurements of thermal performance can be taken, our primary means of evaluating device performance is by measuring the electron tunneling current across the electrodes of prototype devices. Figure 4 (below) shows an I-V curve for a recent prototype.

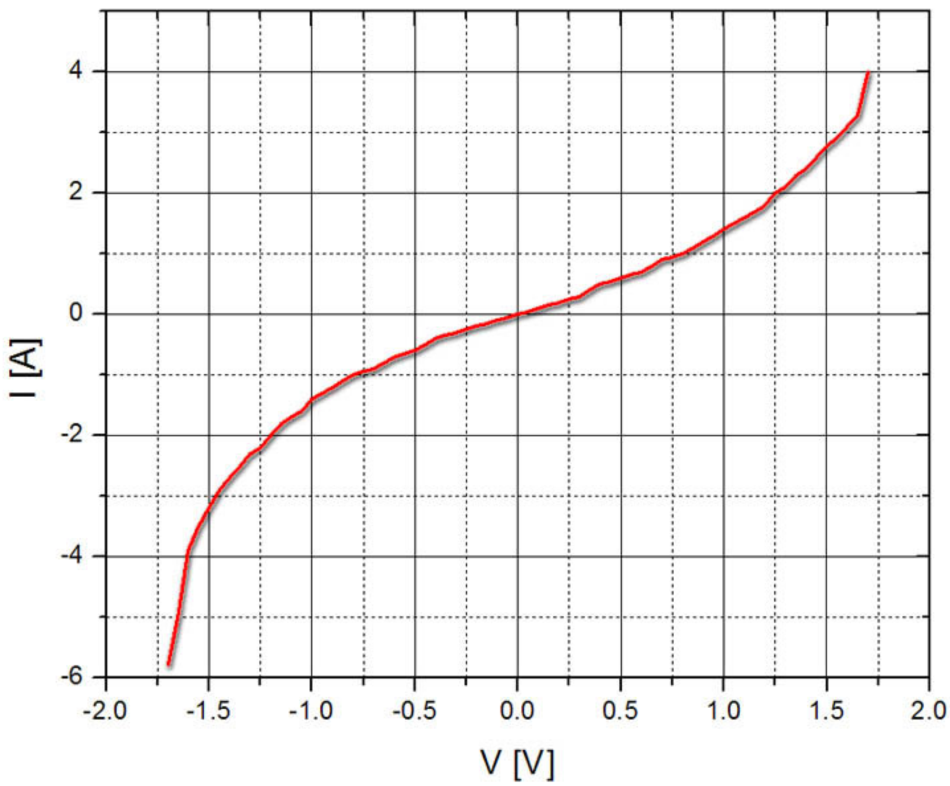


FIGURE 4. I-V Curve of Recent Prototype Showing Current vs. Voltage. Non-linearity Indicates Current from Tunneling as Opposed to Linear Ohmic Current.

Using an I-V curve to compare current (in Amps) to voltage allows us to observe that current passing across the electrodes changes significantly as voltage exceeds the work function of the electrode material. An I-V curve of a system using resistive (Ohmic) current will be linear, rather than the steeply curving graph seen above.

COMPLETING DEVELOPMENT

While earlier prototypes have demonstrated that conformal electrodes can be reliably produced and that electron tunneling occurs, current work is focused on the integration of low work function materials into the electrode surfaces. Work function is defined as the minimum energy required to liberate an electron from an atom. The operating voltage of a working device is determined by the difference in work function between the two electrodes. The ratio of work function between the two electrodes may be varied to produce optimal results depending upon the operating requirements of a particular application.

Our initial efforts towards the integration of low work function materials have involved the incorporation of cesiated thin films on electrode surfaces. Even with our earliest attempts, we have already begun to observe cooling effects in prototypes. Once the integration is complete and performance is optimized, exhaustive calorimetric tests can be conducted to compare actual output and efficiency to theoretically predicted values. Independent theoretical work performed at Stanford University (Hishinuma, 2001) has projected potential cooling output on the order of 5000 Watts/cm^2, although our initial targets are far more modest (3-5 W/cm^2). Based on the availability of funding, we currently anticipate completion of this work in early 2004, with detailed test data to follow shortly thereafter.

PACKAGING AND PRODUCTION

Moving from a laboratory prototype to a production design requires that Cool Chips incorporate necessary spacing and sensing components in a self-contained, modular package. Several designs currently being evaluated include a tube of piezoelectric material surrounding the electrodes, shown in Figure 5 below. This piezoelectric tube acts not only as an actuator to regulate spacing between electrodes, but also acts as a barrier to prevent atmospheric contamination. It is not necessary to maintain high vacuum in this design thanks to an interesting thermal effect: because the spacing between the electrodes is less than the mean free path of the gas molecules present, heat conduction by residual gases is dramatically reduced. Furthermore, by placing the piezo tube outside the primary path for heat conduction, efficiency losses due to thermal backflow are kept to a minimum.

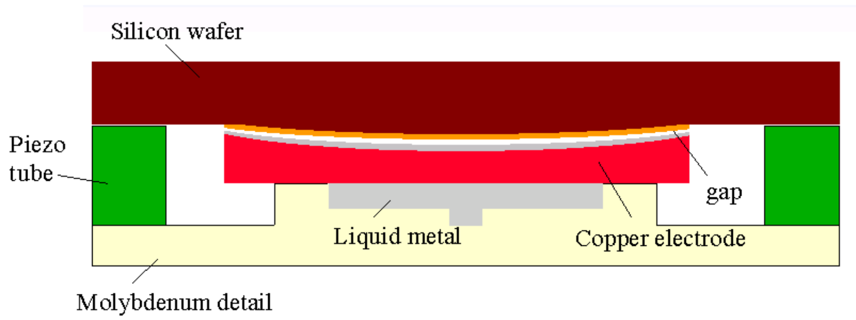


FIGURE 5. Design for a Cool Chip Module Showing Piezoelectric Tube as Both Positioner and Seal.

The actual production process relies on simple techniques well known in the field of semiconductor manufacturing, such as sputtering, chemical vapor deposition (CVD) and electrochemical deposition (ECD). Process step count is low, and materials used are readily available. Because the devices themselves are small, total material cost is kept to a minimum. We expect that mass-produced devices will be cost-competitive with any existing thermal management solution.

CONCLUSION

Laboratory experiments and theoretical work has validated the science of thermotunneling, with tunneling currents in excess of 10A having been measured in prototype devices. Barring any unforeseen technical or financial challenges, remaining development tasks are expected to be completed over the next few months.

Their high efficiency makes Cool Chips an attractive alternative to the thermoelectrics used to cool imaging sensors and electronics packages, regulate shape-memory alloys, and provide temperature control for space suits and habitats. Their precise temperature control and high output make them a candidate to replace cryogenic systems with a compact, lightweight package. Once development is completed, Cool Chips should be an excellent replacement for existing thermal management solutions in many aerospace applications.

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