An all-chromium single electron transistor: A possible new element of single electronics

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The realization of an all-chromium single electron tunneling (SET) transistor is reported. Chromium was chosen as a normal metal with small grain structure forming the oxide layer with a low potential barrier and great chemical and thermal stability. The transistor showed classical I-V curves with an offset voltage of 450 μV and an amplitude of gate modulation of 160 μV. Fitting a tunnel current expression in the experimental I-V curve gave a height of the potential barrier $\phi=170$ meV and a width of the barrier $d=16$ Å. The SET transistor showed a charge sensitivity of 7×10^{-4} $e/\mathrm{Hz}^{1/2}$ at 10 Hz. © *1996 American Institute of Physics.* [S0003-6951(96)03220-2]

A new class of devices based on single charge tunneling phenomena has been intensively developed in recent years (see Refs. 1 and 2 for reviews). These devices operate at low temperatures T and comprise tunnel junctions with a small capacitance $C \gg e^2/k_B T$, where e is the electron charge. The devices have demonstrated unique properties, including sub-electron charge sensitivity, the possibilities of manipulating electrons one by one, and of creating a current standard. However, the main drawback of such devices is their instability due to the shift of a background charge. Several attempts have already been made to eliminate this instability by fabricating SET transistors on various substrates (Si, SiO_2 and Al_2O_3)[3] and by using different electrode materials[4] but have not met with much success. It is clear that testing new materials for tunnel junctions and substrates could be very useful in bringing about an improvement of the noise properties of these devices. Another purpose is to find a normal metal instead of the commonly used superconducting aluminum, in which case we do not need to suppress the superconductivity by a magnetic field. We decided to use chromium for several reasons. This material showed very good stability, excellent adhesion properties, and small grain structure when we used very thin (6 nm) films of Cr as resistors.[5] Chromium forms a stable oxide layer which can be used for the fabrication of tunnel junctions.[6] The low potential barrier between the chromium oxide and other materials leads to comparatively thicker oxide barrier for the same tunnel resistance, and, so, to a smaller capacitance for the same dielectric constant, and probably to more stable junctions. The purpose of this work was to fabricate SET transistors using $Cr–Cr_2O_3–Cr$ tunnel junctions and investigate the parameters of the tunnel barrier and noise properties of the transistors.

The $Cr–CrO_x–Cr$ tunnel junctions were fabricated using electron beam lithography and shadow evaporation technique. We used a double-layer resist composed of PMMA and copolymer (PMMA-PMAA) for an e-beam mask as for Al junctions. However, we had difficulty with the evaporation of Cr as its melting point is higher than that of Al. When the total thickness of evaporated Cr was 50 nm, the mask cracked and samples could not be fabricated successfully. We then reduced the thickness of both electrodes and evaporated the top one in several steps. The base Cr layer of 10 nm thick was evaporated from a thermal boat at a rate of 0.05 nm/s on an oxidized silicon substrate. The tunnel barrier was formed by thermal oxidation in an oxygen atmosphere at a pressure of 2×10^4 Pa for 15 h at room temperature. The formation of the tunnel barrier was the most important step. For the normal operation of the transistor, one should achieve a junction resistance R high enough so that $R \gg R_Q \equiv h/4e^2 \approx 6.47$ kΩ. For a typical junction area of $S=0.01$ $\mu\mathrm{m}^2$ we could not get a value of the resistance high enough. A longer oxidation time did not result in an increase in resistance. The reason for this is a saturation level of Cr_2O_3 of the order of 1 nm formed at room temperatures.[7] The proper resistance was achieved by reducing the junction area to 0.003 $\mu\mathrm{m}^2$ for transistor configuration. Due to different geometry, the area of single junctions made on the same substrate was not reduced to the same level and all investigations were made for the transistor. The top electrode was 20 nm thick and deposited at the same rate as the base electrode but in two steps with a 5 min interval. Electrical contacts to the chip were made by directly connected pogo pins to Cr contact pads. Such contacts produced some instability in transistor operation. Silver paste on the contact pads helped to create more stable contacts. The measurements were made in a dilution refrigerator at temperatures around 50 mK.

A I-V curve of a Cr transistor is shown in Fig. 1(a). The I-V curve has the classical Coulomb blockade shape of a normal metal transistor. The I-V curve at higher bias voltages referred to one junction is shown in Fig. 1(b). At higher voltages it has a noticeable curvature that was not observed for Al junctions. The reason for this curvature is the suppression of the tunnel barrier at voltages lower than for Al due to the lower potential barrier for Cr tunnel junctions. The parameters of the potential barrier, the height φ and the width d, were determined from the I-V curve at higher bias volt-

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